the specification to correspond to the drawing changes and to correct a couple of minor errors discovered therein. It is respectfully submitted that no new matter has been added.

The Examiner has objected to the title. Accordingly, applicant has changed the title so that now it reads in its entirety "SEMICONDUCTOR DEVICE INCLUDING TWO DIES."

Claims 1-4 stand rejected under 35 USC §112, second paragraph, as being indefinitely for failing to particularly point out and distinctly claim the subject matter that applicant regards as the invention. The Examiner indicated that it is not clear what is meant by "source attach area," "gate attach area," and "lead rail." It is respectfully submitted that as clearly described in the specification and indicated in the figures, the leadframe includes on one side, a first source attach area and a first gate attach area (reference signs 20 and 25), as well as a second source attach area and a second gate attach area (reference signs 22 and 24). As can be seen in figure 3, the areas are on opposite sides of the leadframe and a top die is coupled to the first source and gate attach areas on a first surface of the leadframe, while the second die is coupled to the second source attach area and second gate area on a second surface of the lead frame. Thus, it is respectfully submitted that these terms within the claims are definite and that one skilled in the art would understand the scope of applicants' invention. Accordingly, it is respectfully requested that the rejection be withdrawn.

Claims 1 and 4 stand rejected under 35 USC §103(a) as being obvious over Cheah (U.S. Patent No. 6,040,626) in view of Tandy (U.S. Patent No. 5,986,209).

Claims 2 and 3 stand rejected under 35 USC §103(a) as being obvious over Cheah et al. in view of Tandy and Kinsman (U.S. Patent No. 5,789,803).

These rejections are respectfully traversed and reconsideration is respectfully requested.

In the rejection of the claims, the Examiner indicates that Tandy discloses a semiconductor device that includes two dies. The Examiner relies upon figures 2 and 5. However, figures 2 and 5 are directed to multiple semiconductor packages stacked atop

one another with their leads coupled to each other. This is clearly indicated in the brief description of the drawings, as well as at column 1, lines 49-57; and column 4, lines 6-37.

In contrast thereto, and as clearly recited in claim 1, the present invention is directed to a semiconductor device comprising a leadframe, at least two dies, a first of which is coupled to first source and gate attach areas of the leadframe and a second of which is coupled to second source and gate attach areas of the leadframe, and a body, the body being coupled to the semiconductor device such that a drain region of the second die is exposed. None of these features are disclosed or even suggested in either reference and therefore, the combination of the two references do not obviate claim 1.

Accordingly, it is respectfully submitted that claim 1 is allowable. Claims 2-4 depend on claim 1 and therefor, claims 2-4 are allowable for at least the reasons claim 1 is allowable.

Furthermore, with regard to claim 4, it is respectfully submitted that with reference to figure 3, which the examiner relies upon, a drain clip, as corresponds to element 52, is not disclosed in either reference. Furthermore, lead rail, as depicted with reference sign 53 in the figures, is also not disclosed in either reference. Indeed, Cheah refers to element 28 as "a strap member" that is employed to electrically couple the metalized region 18 to the semiconductor die 16. (See column 3, lines 42-44). It clearly does not disclose a drain clip and a lead rail adjacent an edge of the drain clip. Accordingly, claim 4 is allowable for these additional reasons.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

The paragraph beginning at page 2, line 9, has been amended as follows:

Figure 2 is a bottom perspective view of a semiconductor device in accordance with the present invention; [and]

The paragraph beginning at page 2, line 11, has been amended as follows:

Figure 3 is an exploded view of a semiconductor device in accordance with the present invention[.]; and

The paragraph beginning at page 2, line 26, has been amended as follows:

In accordance with a preferred embodiment of the present invention, dies 30, 32 are bumped dies, which are one-piece items. As can be seen in Figure 4, a bumped die includes the die, an "under bump" material 40 that serves as an intermediate layer between the top surface of the die and solder bump 41[, and solder bumps 41 themselves]. Preferably, the under bump material is one of TiW, Cu, Au or an equivalent. In the example illustrated in Figure 4, the under bump material is broken into three layers - Cu plating 40a, sputtered Cu 40b, and sputtered Ti 40c.

The paragraph beginning at page 3, line 1, has been amended as follows:

A drain clip assembly 50 is attached to drain region 51 of the first die preferably with solder. The drain clip assembly includes a top die drain clip 52 and a side rail leadframe 53. Solder paste is dispensed on the drain region of the first die and into elongated v-groove 54 in side rail 53. Clip [50]52, preferably comprising copper, is supplied, (preferably in reel form) and pick-and-placed onto the die backside such that edge 55 of the copper clip is placed within the elongated v-groove. Thus, the clip provides contact with the first die's drain regions and couples these drain regions to leads 56 of the side rail.

The paragraph beginning at page 3, line 15, has been amended as follows:

As can be seen in Figure 1, leads 62 serve as the common source connections while leads 56 serve as the drain connections for the first or top die. Lead [63]12a serves as the gate connection for the first die while lead [64]12b serves as the gate connection for the second die. Parallel connection of the top and bottom dies may be specially routed on the circuit board for optimum electrical performance. Isolating the connections of the top and bottom dies may be an option depending upon the device application.

IN THE TITLE:

The title has been amended as follows:

[DUAL STACKED DIE PACKAGE]SEMICONDUCTOR DEVICE WITH TWO DIES